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First Named Inventor:	HOGERTON, PETER B.		
Application No.:	09/690600	Group Art Unit:	2827
Filed:	October 17, 2000	Examiner:	Luan C. Thai
Title:	SOLVENT ASSISTED BURNISHING OF PRE-UNDERFILLED SOLDER-BUMPED WAFERS FOR FLIPCHIP BONDING		

BRIEF ON APPEAL

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Sep. 24, 2004 Susan P. Gumatz
Date Signed by: Susan P. Gumatz

Dear Sir:

This is an appeal from the Office Action mailed on March 25, 2004, in light of the Advisory Action mailed May 27, 2004, finally rejecting claims 16-19.

A Notice of Appeal in this application was mailed on July 23, 2004, and was received in the USPTO on July 26, 2004.

The fee required under 37 CFR § 41.20(b)(2) for filing an appeal brief should be charged to Deposit Account No. 13-3723.

Appellants request the opportunity for a personal appearance before the Board of Appeals to argue the issues of this appeal. The formal request and fee for the personal appearance will be timely paid after receipt of the Examiner's Answer or Supplemental Examiner's Answer.

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REAL PARTY IN INTEREST

The real party in interest is 3M Company of St. Paul, Minnesota and its affiliate 3M Innovative Properties Company of St. Paul, Minnesota.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1-15 and 20-23 were withdrawn by the Examiner after a restriction requirement.

Claims 16-19 have been finally rejected.

Claims 16-19 are the claims on appeal.

STATUS OF AMENDMENTS

An amendment to claim 16, which corrected a typographical error, was filed after the final rejection. The Examiner entered this amendment. (Advisory Action mailed May 27, 2004, page 1, ¶ 7.)

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 16 provides an integrated circuit chip **420** comprising a bumped side having a passivation surface **422** on which a plurality of conductive bumps **424** are disposed. (Page 23, lines 3-8; and FIGS. 15c and 16c.) The conductive bumps **424** are selected from the group consisting of: solder, meltable solid metals, gold, electroless nickel, electroless gold, and combinations thereof. (Page 11, lines 8-10.) The conductive bumps **424** are metallurgically bonded to integrated circuit chip **420**. (Page 1, line 30 – page 2, line 1; and page 2, lines 17-20.)

The integrated circuit chip **420** of claim 16 further comprises a layer of adhesive **426** that covers the bumped side of the integrated circuit chip, the adhesive **426** having a primary surface **430** that is substantially parallel to the passivation surface **422**. (Page 23, lines 12-14.) The conductive bumps **424** have exposed contact regions **436** that are not covered by the adhesive **426**, wherein the exposed contact regions **436** of the conductive bumps **424** have a rounded profile. (Page 23, lines 15-17; page 24, lines 1-3.) See also, e.g., page 7, lines 4-10.

The following additional information is provided as an aid to understanding the claimed invention. Support for this information may be found at pages 1-5 of Applicants' specification.

The vast majority of electronic circuit assemblies in the world today use integrated circuit (IC) chips, which have been housed in protective packages. One technique used to reduce circuit size and improve performance involves attaching IC devices directly to a substrate using perimeter or area arrays of solder balls mounted on the face of a chip. By inverting or "flipping" the chip such that these solder balls are placed in contact with pads on the substrate and passing the entire assembly through a solder reflow process, the IC may be metallurgically bonded to the substrate.

Typically, a finished flip-chip assembly must maintain electrical continuity throughout the lifetime of the device. Mismatches of both the coefficient of thermal expansion and the elastic modulus between the silicon IC and the substrate (e.g., a printed circuit board) generate high stresses in the contact joints when the circuit is passed through thermal excursions. These stresses can lead to solder joint fatigue failure after repeated temperature cycles.

An important breakthrough has been the development of the underfill process, which uses a high-modulus curable adhesive to fill the empty space between the solder balls under the chip so that the stress in the joint is shared by the adhesive and distributed more evenly across the

entire interface as opposed to being concentrated at the perimeter balls. The use of an "underfill' adhesive has enabled flip-chip technology to be applied to a broader range of assemblies.

A reliable solder flip-chip method of IC interconnect is just beginning to be applied to organic substrates. Significant processing and materials challenges are slowing this technology in spite of strong demand from designers. The current flip-chip assembly process has too many steps, is too costly and is not extendable to future IC designs. A simplified flip-chip assembly process that reduces cost and demands from the underfill adhesive systems will enable flip-chip assembly to become a more broadly attractive approach for circuit assembly.

The present invention provides an integrated circuit chip useful in a simplified flip-chip assembly process. (See, e.g., claim 16, described above.)

Grounds of Rejection to be Reviewed on Appeal

I. Claims 16-19 stand rejected under 35 U.S.C. §103(a) as purportedly being obvious over Matsubara et al. (JP-402023623A) ("Matsubara") in combination with JP-07130749A ("JP-749")

II. Claims 16-19 stand rejected under 35 U.S.C. §103(a) as purportedly being obvious over Matsubara in combination with Yeh et al. (U.S. 5,607,099) ("Yeh").

Argument

I. Claims 16-19 stand rejected under 35 U.S.C. §103(a) as purportedly being obvious over Matsubara et al. (JP-402023623A) ("Matsubara") in combination with JP-07130749 ("JP-749").

A. The Examiner improperly ignored the phrase "metallurgically bonded" when assessing the patentability of claim 16.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. See *In re Royka*, 490 F.2d 981; 180 U.S.P.Q. 580 (CCPA 1974). Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385; 165 U.S.P.Q. 494, 496 (CCPA 1970). (See also MPEP § 2143.03.)

In part, the present invention provides an integrated circuit chip comprising a bumped side having a passivation surface on which a plurality of conductive bumps is disposed. The conductive bumps are metallurgically bonded to the integrated circuit chip. (Claim 16, emphasis added.) Such a bond structure can be formed by, e.g., an elevated temperature solder reflow process (see, e.g., page 1, line 28 to page 2, line; page 2, lines 17-20; and page 7, lines 4-6). The conductive bumps have exposed contact regions having a rounded profile that are not covered by the adhesive. (See, e.g., claim 16.)

In the Final Office Action mailed March 25, 2004, the Examiner acknowledged the "metallurgically bonded" limitation asserting that it "raise[d] new issues that would require further consideration and/or search." (See, e.g., Office Action mailed March 25, 2004, page 7, ¶ 7.) As evidenced by the inclusion of a PTO-892 form listing new art, the Examiner conducted such a search. Furthermore, the Examiner applied new references (e.g., Yeh) in rejecting claims 16-19, which purportedly addressed the "metallurgically bonded" limitation. (See, Office Action mailed March 25, 2004, ¶ 3 at pages 5-7. See also page 7, ¶ 5.)

In response to Applicants' evidence that a *prima facie* case of obviousness had not been established, the Examiner reversed course and asserted that the previously considered limitation of metallurgically bonded was a product-by-process limitation, which need not be considered. (Advisory Action mailed May 27, 2004.)

1. "Wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" is a structural limitation.

The complete text of claim 16 is presented below, so that the limitation in dispute, which has been italicized, may be seen in its full context.

16. An integrated circuit chip comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed, wherein the conductive bumps are selected from the group consisting of: solder, meltable solid metals, gold, electroless nickel, electroless gold, and combinations thereof, and *wherein said conductive bumps are metallurgically bonded to said integrated circuit chip*; and

a layer of adhesive that covers the bumped side of the integrated circuit chip, the adhesive having a primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

Applicants respectfully submit that the phrase "wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" describes a structural limitation.

"[W]ords of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and by default interpreted in their structural sense, unless the patentee has demonstrated otherwise." 3M Innovative Properties Co. v. Avery Dennison Corp., 350 F.3d 1365, 1371; 69 U.S.P.Q.2d 1050, 1055 (CAFC 2003). For example, in *In re Garnero*, the court held that the limitation "expanded perlite particles which are interbonded one to another by interfusion," should be construed as a structural limitation and not a product-by-process limitation. 412 F.2d 276, 278-79; 162 U.S.P.Q. 221, 223 (CCPA 1976) (emphasis added). The court further noted that the terms "'intermixed,' 'ground in place,' 'press fitted,' 'etched,' and 'welded' all ... at one time or another have been separately held capable of construction as structural, rather than process, limitations." *In re Garnero*, 412 F.2d at 279; 162 U.S.P.Q. at 223.

Applicants further submit that one of ordinary skill in the relevant art would understand that the limitation "wherein said conductive bumps are metallurgically bonded to said integrated

circuit chip" does not describe a process, but rather an end result of well-known processes such as, e.g., soldering. For example, Applicants' specification describes soldering processes that provide a metallurgically bonded structure. (See, page 1, line 30 – page 2, line 1; and page 2, lines 17-25.) In addition, see Surface Mount Technology: Principles and Practice; Prasad, R.P., Van Nostrand Reinhold, NY (1989) pp. 349 and 423; already of record (submitted May 18, 2004, with Applicants' response to the Final Office Action); which describes solderable connections as providing "good metallurgical bonds."

For at least the foregoing reasons, the limitation "wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" of claim 16 should be regarded as a structural, and not a process, limitation. The Examiner is not free to selectively ignore claimed features or to dismiss them with conclusory statements that they are process features. Rather, the law requires the Examiner to show how each limitation of claims 16-19 is described, taught, or suggested by the prior art. See, e.g., *In re Royka*, 490 F.2d 981; 180 U.S.P.Q. 580 (CCPA 1974). The Examiner has failed to meet this legal obligation and, failing to do so, has failed to establish a *prima facie* case of obviousness. Therefore, the Board should reverse this rejection.

2. Assuming, *arguendo*, the phrase "wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" is treated as a product-by-process limitation, the resulting product comprises a metallurgical bond.

A product-by-process claim is proper. *In re Luck*, 476 F.2d 650, 653; 177 U.S.P.Q. 523, 525 (CCPA 1973). (See also MPEP § 2173.05(p).). When assessing the patentability of a product-by-process claim over the prior art, the structure implied by the process steps should be considered. See *In re Hughes*, 496 F.2d 1216, 1218; 182 U.S.P.Q. 106, 108 (CCPA 1974); and *In re Bridgeford*, 357 F.2d 679, 682-83; 149 U.S.P.Q. 55, 57-58 (CCPA 1966). (See also MPEP § 2113.)

Assuming, *arguendo*, that the limitation "wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" is treated as a product-by-process limitation; Applicants respectfully submit that one of ordinary skill in the relevant art would understand that the formation of a metallurgical bond is inherent, if not explicit, in a process described by the phrase "metallurgically bonded." Applicants further submit that one of ordinary skill in the relevant art would immediately envisage the formation and existence of a

metallurgical bond between a conductive bump and a integrated circuit chip that are "metallurgically bonded." (See, e.g., Applicants' specification at page 1, line 30 – page 2, line 1; and page 2, lines 17-25; and Surface Mount Technology: Principles and Practice; Prasad, R.P., Van Nostrand Reinhold, NY (1989) pp. 349 and 423.)

Therefore, the structure (i.e., a metallurgical bond) implied by the purported process step (i.e., metallurgically bonded) must be considered when assessing the patentability of claims 16-19. As such, the Examiner is required to show how this structure, in conjunction with the remaining limitations of claims 16-19, is described, taught, or suggested by the prior art. The Examiner has failed to do so and, thus, has failed to establish a *prima facie* case of obviousness.

In summary, Applicants respectfully submit that interpreting the phrase "wherein said conductive bumps are metallurgically bonded to said integrated circuit chip" as a structural limitation is in accord with Federal Circuit practice. In addition, such a reading is consistent with the interpretation one of ordinary skill in the art would apply to this phrase. However, even if the phrase were interpreted as a product-by-process limitation, the claim still must be read as including the presence of a metallurgical bond between the conductive bumps and the integrated circuit chip, as such a structure is clearly implied.

B. The Examiner's proposed combination is contrary to the express teachings of the references.

A reference that "teaches away" from the claimed invention is a significant factor to be considered in obviousness. *In re Gurley*, 27 F.3d 551, 552; 31 U.S.P.Q.2d 1130, 1132 (Fed. Cir. 1994). (See also MPEP §2145(X)(D)(1).) It is improper to combine references where the references teach away from their combination. See, *In re Grasselli*, 713 F.2d 731, 744-45; 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); and *In re Sponnable* 405 F.2d 578, 587; 160 U.S.P.Q. 237, 244 (CCPA 1969). (See also MPEP §2145(X)(D)(2).)

As discussed, JP-749 describes a process for forming stud bumps on an electrode involving the following steps. First, a spherical piece of metal is formed at the tip of a capillary tube. Next, the sphere is brought into contact with the electrode and deformed to form a nail head or stud bump. The metal is adhered to the electrode by ultrasonic sticking-by-pressure (e.g.,

thermocompression bonding, or ultrasonic thermocompression bonding). (See, e.g., [0029] – [0046], and Drawings 3-5.)

In contrast, Matsubara describes a method of bonding wherein an adhesive layer is formed over the main bodies of the electrode. Subsequently, conductive particles are adhered to the adhesive layer while the adhesive layer has tackiness, and portions of the particles form protrusions from the adhesive (i.e., "bump electrodes"). The adhesive is then used to bond the circuit boards together. (Page 4, line 34 – page 5, line 9. See also page 8, lines 9-17.)

The Examiner has failed to show how this well-known method of adhesive bonding results in the formation of a metallurgical bond. In fact, Matsubara explicitly discussed metal to metal bonding noting that this requires the electrodes to be made of a material having an affinity for the bump material (e.g., gold) and that such connections are **poor**. (Page 3, lines 19-26, emphasis added.) Matsubara purports to provide a new method of bonding a chip to a board, which uses an adhesive layer that would overcome these problems. (See, page 4, lines 18-281.) Thus, Matsubara expressly teaches away from the method and resulting structures of JP-749.

In addition, the method of Matsubara is characterized by including a process during which an adhesive layer is formed over the main body of an electrode. (Page 4, lines 25-27.) Subsequently, conductive particles are adhered to the adhesive layer. (Page 4, lines 34-36.) The Examiner has not shown how to overcome the adhesive applied over the main body of the electrode (as required by Matsubara), which would prevent a metal sphere from being brought into pressure contact with the electrode, as required by JP-749. (See, e.g., Paragraphs [0042] – [0052]; and Drawings 3-5.)

In summary, the Examiner's proposed combination of Matsubara and JP-749 contradicts the express teachings of both references. The Examiner has shown no teaching, suggestion or motivation in the art that would lead one of ordinary skill in the art to ignore these express teachings. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness. For at least these reasons, the rejection of claims 16-19 under 35 USC § 103(a) as purportedly being unpatentable over Matsubara et al. (JP-402023623A) in view of Japanese patent JP-07130749A is unwarranted and should be reversed.

C. The Examiner has failed to show an enabling combination of references.

"References relied upon to support a rejection under 35 USC 103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. An invention is not 'possessed' absent some known or obvious way to make it." *In re Payne*, 606 F.2d 303, 314; 203 U.S.P.Q. 245, (CCPA 1979) (internal citations omitted).

The present invention provides in part an integrated circuit chip comprising a bumped side having a passivation surface on which a plurality of conductive bumps are disposed. The conductive bumps are metallurgically bonded to the integrated circuit chip. A layer of adhesive covers the bumped side of the integrated circuit chip, the adhesive having a primary surface that is substantially parallel to the passivation surface. The conductive bumps have exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile. (See claim 16.)

As discussed, the process described by Matsubara is characterized by forming an adhesive layer over the main body of an electrode prior to the introduction of conductive particles. (Page 4, lines 25-36.) According to the Examiner, JP-749 describes metallurgically stabilized bonding, and asserts that it would have been obvious to apply these "teachings" to Matsubara's device. (Office Action mailed March 25, 2004, page 4.)

At best, JP-749 may describe the desirability of metallurgical bonds in some applications. As discussed, JP-749 describes only one method of achieving such a bond. This method requires bringing a sphere of metal into contact with the electrode where the metal is adhered to the electrode by ultrasonic sticking-by-pressure (e.g., thermocompression bonding, or ultrasonic thermocompression bonding). (See, e.g., [0029] – [0046], and Drawings 3-5.)

The Examiner has not shown how the method of JP-749, which requires direct contact between the sphere of metal and the electrode could be possible in the presence of an adhesive layer over the main body of the electrode, as described by Matsubara. In addition, the Examiner has acknowledged that Matsubara fails to teach conductive bumps that are metallurgically bonded in combination with an adhesive layer. (Office Action mailed March 25, 2004, page 4.) The Examiner has failed to provide any other source for a description, teaching, or suggestion of the formation of metallurgical bonded bumps having an exposed rounded profile in combination with an adhesive layer covering the bumped surface of an IC, as required by the present

invention. For at least these reasons, the references fail to "place the claimed invention in the possession of the public" and, thus are non-enabling and fail to provide an acceptable basis for a rejection under 35 U.S.C. § 103. (*In re Payne*, 606 F.2d 303, 314; 203 U.S.P.Q. 245, (CCPA 1979).)

D. The Examiner has failed to show how the prior art describes, teaches, or suggests all elements of the claimed invention.

As discussed, regardless of whether the phrase "metallurgically bonded" is interpreted as a structural limitation or a product-by-process limitation, claim 16 requires the presence of a metallurgical bond between the conductive bumps and the integrated circuit chip. Thus, to establish a *prima facie* case of obviousness, this limitation, *inter alia* must be taught or suggested by the prior art. See, e.g., *In re Royka*, 490 F.2d 981; 180 U.S.P.Q. 580 (CCPA 1974).

In addition to a metallurgical bond, the present invention requires that the conductive bumps have exposed contact regions having a rounded profile. (See, e.g., claim 16.) As discussed in the specification, in some embodiments, retaining the rounded profile allows easier deformation of the bumps, which may provide, e.g., reduced stand off, better adhesive wetting and encapsulation, and a better bond between the IC chip and the substrate. (Page 24, lines 3-10.)

The Examiner explicitly acknowledged that Matsubara fails to teach conductive bumps that are metallurgically bonded to the integrated circuit chip. (Office Action mailed March 25, 2004, pages 4 and 6; and Advisory Action mailed May 27, 2004, page 2.) The Examiner asserted that JP-749 teaches a metallurgically stabilized bond formed by pressure welding. The Examiner further asserted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the JP-749 teachings to Matsubara's device in order to reduce damage on the joining part. (Office Action mailed March 25, 2004, page 4.)

JP-749 describes a method for forming stud bumps (nail head bumps). (See [0040], [0045], and Drawings 3-5.) As described by JP-749, spherical metal ball **15**, attached to capillary tube **3** is brought into contact with electrode pad **7a** of IC chip **7**. Capillary tube **3** is then lifted from the IC chip, deforming the metal ball in to the shape of a nail heading ball bump **16**. The nail head shaped bump (element **16** in Drawings 3-5) is required by JP-749, so that the tip of the nail head bump can engage with feed-hole **14a** of the inner lead **14** of TAB film **13**, as shown in Drawing 5.

Based on the foregoing, Applicants respectfully submit that JP-749 fails to describe, teach, or suggest conductive bumps having a rounded profile in an integrated circuit chip. In fact, JP-749 explicitly teaches away from such structures, as they would be incompatible with JP-749's teaching that the nail head bump engages the feed-holes of a TAB film.

Thus, assuming, *arguendo*, there was proper motivation "to apply the JP-749 teachings to Matsubara's device," as proposed by the Examiner, and one come overcome the incompatible process differences, the combination of JP-749's nail-head bumps with Matsubara still would not describe, teach, or suggest all of the elements of the claimed invention.

Because the Examiner has failed to show how Matsubara in combination with JP-749 teaches all of the limitations of the claimed invention, the Examiner has failed to establish a *prima facie* case of obviousness. (See, e.g., *In re Royka*, 490 F.2d 981; 180 U.S.P.Q. 580 (CCPA 1974); and *In re Wilson*, 424 F.2d 1382; 165 U.S.P.Q. 494 (CCPA 1970). See also MPEP § 2143.03.) For at least these reasons, the rejection of claims 16-19 as purportedly being unpatentable under 35 U.S.C. §103(a) over Matsubara in combination with JP-749 should be reversed.

E. Conclusion

The combination proposed by the Examiner (i.e., to combine the stud bumps of JP-749 with the adhesive coated chip of Matsubara) would require one of ordinary skill in the art to ignore the express teachings to the Matsubara. In addition, the application of the stud bumps to the adhesive coated substrate of Matsubara would be contrary to the teaching of JP-749, which requires the metal ball to contact the electrodes. Also, the references fail to enable one of ordinary skill in the art to form an IC having the requisite metallurgically bonded bumps with exposed rounded profiles in combination with an adhesive covering the bumped side of the IC. Finally, even if the Examiner's proposed combination were attempted, and the processing contradictions could be overcome, the construction resulting would not have bumps with a rounded profile, and thus would not describe, teach, or suggest all the limitations of the claimed invention. Therefore, for at least these reasons, the rejection of claims 16-19 under 35 USC § 103(a) as being unpatentable over Matsubara et al. (JP-402023623A) in view of Japan patent JP-07130749A (JP-749) is unwarranted and should be reversed.

II. Claims 16-19 stand rejected under 35 U.S.C. §103(a) as purportedly being obvious over Matsubara in combination with Yeh et al. (U.S. 5,607,099) ("Yeh").

As discussed, the Examiner has acknowledged that Matsubara fails to teach conductive bumps that are metallurgically bonded to an integrated circuit chip. (See, e.g., Office Action mailed March 25, 2004, page 6.) The Examiner asserts that a conductive bump being metallurgically bonded to an integrated circuit chip is conventionally applied in semiconductor art as taught by Yeh. The Examiner further asserts that it would have been obvious to apply the metallurgical bonding process to Matsubara. (Office Action mailed March 25, 2004, page 6.) Applicants respectfully traverse this combination.

First, Yeh describes a method of forming solder bumps on a carrier and transferring the bumps to a circuit chip. (Col. 2, lines 32-35.) Matsubara discussed the deficiencies of solder bump transfer methods such as those described by Yeh (page 3, lines 9-25) and purports to provide a process which overcomes these deficiencies. (Page 3, lines 26-31). Thus, Matsubara expressly teaches away from the method and resulting structures of Yeh. Applicants respectfully submit that the Examiner has failed to present any teaching, suggestion or motivation in the art that would lead one of ordinary skill in the art to ignore Matsubara's explicit teaching and combine the references as suggested.

Second, as shown in FIG. 1, and described by Yeh at col. 5, lines 14-26, the formation of a metallurgical bond between solder ball and the flip chip requires the molten solder to wet and transfer to the flip chip. In contrast, the process of Matsubara requires an adhesive layer over the electrode prior to the introduction of the conductive particles. (Page 4, lines 25-26.) Applicants respectfully submit that the adhesive layer of Matsubara would prevent the solder balls of Yeh from contacting and wetting the electrodes, thus destroying the functionality of Yeh. Alternatively, in order to maintain the functionality of Yeh, one of ordinary skill in the relevant art would have to ignore the express teaching of Matsubara that the electrodes be covered by a layer of adhesive.

Third, the Examiner has not shown where the combination of Matsubara and Yeh is enabling. As Yeh requires contact and wetting of the electrodes by the solder balls, and Matsubara requires the formation of an adhesive layer over the electrodes, the Examiner has not shown how one of ordinary skill in the art could not combine the teachings of Yeh and

Matsubara to achieve both metallurgically bonded bumps and an adhesive covering the bumped surface.

In summary, the Examiner has not shown that Matsubara and Yeh can be combined to achieve all elements of the claimed invention without ignoring the express teachings of the references, and/or destroying the functionality of one or both references. In addition, the proposed combination fails to enable one of ordinary skill in the art to make all elements of the claimed invention. For at least these reasons, the Examiner has failed to establish a *prima facie* case of obviousness. Therefore, the rejection of claims 16-19 under 35 USC § 103(a) as purportedly being unpatentable over Matsubara et al. (JP-402023623A) in view of Yeh (U.S. Patent No. 5,607,099) is unwarranted and should reversed.

CONCLUSION

For the foregoing reasons, Applicants respectfully submit that the Patent Office has not met the initial burden of a *prima facie* case of obviousness, and thus has erred in rejecting this application under 35 USC § 103(a). Applicants respectfully request reversal of each of the rejections.

Respectfully submitted,

24 Sept 2004
Date

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CLAIMS APPENDIX

1. (withdrawn) A method for connecting an integrated circuit chip to a circuit substrate, the integrated circuit chip including a bumped side having a plurality of conductive bumps, the method comprising the steps of:

applying adhesive directly to the bumped side of integrated circuit chip;

removing portions of the adhesive to expose contact regions of the conductive bumps, wherein the portions of adhesive are removed by softening the adhesive with a solvent and wiping the softened adhesive from the conductive bump; and

placing the bumped side of the integrated circuit chip against the circuit substrate such that the bumps provide for an electrical connection between the integrated circuit chip and the circuit substrate, and the adhesive forms a bond between the integrated circuit chip and the circuit substrate.

2. (withdrawn) The method of claim 1, wherein after removing the portions of adhesive, the exposed contact regions of the conductive bumps have a rounded profile.

3. (withdrawn) The method of claim 1, wherein after removing the portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

4. (withdrawn) The method of claim 1, wherein a portion of the adhesive is removed to create an offset between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

5. (withdrawn) The method of claim 1, wherein the adhesive is applied to the integrated circuit chip by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the integrated circuit chip.

6. (withdrawn) The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

7. (withdrawn) The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

8. (withdrawn) A method for manufacturing integrated circuit chips comprising the steps of:

providing a wafer including a bumped side having a plurality of conductive bumps;

applying adhesive to the bumped side of the wafer, such that the conductive bumps are over-coated with adhesive.;

softening the adhesive with a solvent;

wiping the softened adhesive from the tips of the over-coated conductive bumps to expose contact regions of the conductive bumps; and

dicing the wafer on which the adhesive has been applied into individual integrated circuit chips.

9. (withdrawn) The method of claim 8, wherein after wiping the softened adhesive from the tips of the over-coated conductive bumps, the exposed contact regions of the conductive bumps have a rounded profile.

10. (withdrawn) The method of claim 8, wherein the adhesive is applied to the wafer by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the wafer.

11. (withdrawn) The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

12. (withdrawn) The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

13. (withdrawn) The method of claim 8, wherein after removing the overcoat portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

14. (withdrawn) The method of claim 8, wherein after removing the overcoat portions of the adhesive, an offset exists between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

15. (withdrawn) The method of claim 8, wherein after the overcoat portions of adhesive are removed, and prior to dicing the wafer, a protective cover is placed over the adhesive and exposed contact regions.

16. (previously presented) An integrated circuit chip comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed, wherein the conductive bumps are selected from the group consisting of: solder, meltable solid metals, gold, electroless nickel, electroless gold, and combinations thereof, and wherein said conductive bumps are metallurgically bonded to said integrated circuit chip; and

a layer of adhesive that covers the bumped side of the integrated circuit chip, the adhesive having a primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

17. (original) The integrated circuit chip of claim 16, wherein the primary surface of the adhesive is polished.

18. (original) The integrated circuit chip of claim 16, wherein the conductive bumps have heights greater than a thickness of the adhesive.

19. (original) The integrated circuit chip of claim 16, wherein portions of the conductive bumps project outward from the primary surface of the adhesive such that a stand-off

exists between the rounded profile of the conductive bumps and the primary surface of the adhesive.

20. (withdrawn) A plurality of integrated circuit chips in wafer form comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed; and

a layer of adhesive that covers the bumped side of the circuit substrate, the adhesive having an primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

21. (withdrawn) The plurality of integrated circuit chips in wafer form of claim 20, wherein the primary surface of the adhesive is polished.

22. (withdrawn) The plurality of integrated circuit chips in wafer form of claim 20, wherein the conductive bumps have heights greater than a thickness of the adhesive.

23. (withdrawn) The plurality of integrated circuit chips in wafer form of claim 20, wherein portions of the conductive bumps project outward from the primary surface of the adhesive such that a stand-off exists between the rounded profile of the conductive bumps and the primary surface of the adhesive

EVIDENCE APPENDIX

Surface Mount Technology: Principles and Practice; Prasad, R.P., Van Nostrand Reinhold, NY (1989) pp. 349 and 423.

Submitted May 18, 2004, with Applicants' response to the Final Office Action.

Entry of this evidence may be inferred from the Examiner's Advisory Action mailed May 27, 2004, which stated, "Applicant's arguments filed on 5/18/04 have been fully considered but they are not persuasive." (Page 2.)

Surface Mount Technology

Principles and Practice

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To my wife Pe
and my childre
the ones who r

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Chapter 10
Metallurgy of Soldering and Solderability

10.0 INTRODUCTION

The solder used in electronic assembly serves to provide electrical and mechanical connections. In through-hole mount assemblies we had to worry primarily about obtaining sound electrical connections, because the plated through holes imparted sufficient mechanical strength. With the advent of SMT, the role of the surface mount solder joint has become very critical, because it must provide both mechanical and electrical connections. The solder joint strength is controlled by the land pattern design and a good metallurgical bond between component and board.

Surface mount land pattern design for providing adequate mechanical strength was covered in Chapter 6. In this chapter we concentrate on the metallurgical aspects of a reliable solder connection, as determined by the solder and the solderability of components and boards. A reliable solder connection must have a solderable surface to form a good metallurgical bond between the solder and the components being joined. An understanding of metallurgical bonding entails knowledge of phase diagrams, the concept of leaching, surface finish, wetting, oxidation of metallic surfaces.

Metallurgical phase diagrams are used to display the solubility limits of one metal into another and the melting temperatures for metals and their alloys, for a better understanding of intermetallic bonds. Phase diagrams can also be used for better understanding of leaching or dissolution phenomenan (of one metal into another). Finally, to produce solder joints in a cost-effective way, we need to know about the methods, requirements, and economics of solderability testing.

The focus of this chapter is on the practical aspects of metallurgical issues related to solderability of surface mount assemblies. The subject of soldering for surface mount assemblies is covered in Chapter 12. For an expanded coverage of basic metallurgical issues in electronics, refer to Wassink [1] and Manko [2].

Chapter 12
Soldering of Surface Mounted Components

12.0 SOLDERING

Welding, brazing, and soldering processes for joining metals together differ basically with respect to the temperature at which the joining takes place. Welding is generally used for joining ferrous metals and is accomplished at high temperatures (1500–2000°F). Brazing is used for joining nonferrous metals at relatively lower temperatures (800–1000°F). Soldering, which is used mostly for electronic products, occurs at the lowest temperatures (400–500°F).

In all cases, either two similar metals are joined, or certain dissimilar metals or alloys. The joining mechanism is governed by the formation of intermetallic compounds between the metals to be joined. A basic knowledge of metallurgical properties and of phase diagrams is necessary for an understanding of the principles involved in joining. The metallurgy of soldering is discussed in Chapter 10. Now we focus on the processes and equipment used in this form of joining.

The earliest electronic products were hand soldered. In the 1950s hand soldering was replaced by the wave soldering process for mass soldering of through-hole components. Then in the 1970s, reflow soldering came into widespread usage for surface mount components. However, for surface mounting, depending on the component mix, both wave and reflow soldering processes are used.

The basic differences between wave and reflow soldering lie in the source of heat and the solder. For example, in wave soldering, the solder wave serves the dual purpose of supplying heat and solder. The source for the supply of solder is unlimited because the wave pot holds more than 500 pounds. In reflow soldering, however, solder paste is applied first in a predetermined quantity, as discussed in Chapter 9, and during reflow, heat is applied to melt (i.e., reflow) the solder paste. Thus a more appro-

First Named Inventor: **HOGERTON, PETER B.**

Case No.: **53434US009**

Application No.: **09/690600**

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Enclosures: **Brief on Appeal**

Amount charged to Deposit Account: **$330.00**

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